

COLOR TV PROCESSING USING INTEGRATED CIRCUITS

by Larry Blaser and Derek Bray*

INTRODUCTION

Within the next two years, the semiconductor industry should have the capability of producing large quantities of monolithic, silicon, integrated circuits (IC's) at prices that will be attractive to the consumer market. Investigation of the various ways these devices can be utilized in consumer equipment is important at this time in view of their low cost, high reliability, and increasing availability.

This paper describes one such use: a solid-state circuit developed for the processing function in a color television receiver. A combination of discrete bipolar transistors and monolithic silicon microcircuits, comprised of bipolar transistors and diffused resistors are used.

During the past years, various vacuum tube circuits have been developed for mass-produced color television receivers. The color processing circuits in all of these receivers have one feature in common: They all rely on the picture tube for final matrixing. Color difference signals are applied to the control grids of a three-gun picture tube, and luminance signals are applied to the cathodes. This system has been used to minimize both short- and long-term drift problems inherent with vacuum tubes.

Because drift problems are greatly reduced with solid-state circuits, it has been interesting to reconsider pre-picture tube matrixing in an R-G-B system, such as the one described in this paper. With this system, color difference signals are matrixed with luminance information prior to the time the video signals are supplied to the picture tube, so that video signals need be applied to only three elements. These elements can be either the three control grids or the three cathodes of the picture tube.

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ADVANTAGES OF AN R-G-B SYSTEM

An R-G-B system, by the use of semiconductor circuitry, offers the following distinct advantages over the picture tube matrix system.

1. Fewer components are required, since luminance and chrominance signals are commonly shared in the output circuitry.
2. Components are less costly. The voltage and power ratings for the video output transistors are lower than the ratings required of the chrominance output devices in the picture tube matrix system. The ratings are much lower than that of the separate luminance output device required in the picture tube matrix system.
3. Power consumption is lower because of the lower dissipation in the video output circuitry.
4. Gray scale tracking adjustments set up correctly compensated color drive for best color fidelity, regardless of relative phosphor efficiencies in the picture tube. (Additional controls, separate from the gray scale tracking controls, would be required for color drive correction in the picture tube matrix system.)
5. Both black-and-white and color performance is better because of the excellent luminance response which can be achieved in the video output circuitry. The luminance response in the picture tube matrix system often suffers because of the high capacitive loading on the luminance output stage. A video output transistor in the R-G-B

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6. A high degree of arc protection for the video output devices is provided. Because only the cathodes are driven, the control grids of the picture are decoupled to ground. Arcs from the picture tube anode are thus bypassed to ground without reaching any of the video output devices.

A block diagram of a completely solid-state R-G-B processing system is shown in Fig. 1. The composite video signal from the detector of the video IF amplifier is fed through a buffer state into: (1) the first luminance amplifier, (2) the chroma bandpass amplifier, and (3) the signal processing circuitry.



Demodulator reference signals are generated in the quadrature amplifier, which also serves as a buffer to the color oscillator. Color difference signals, $E_R' - E_Y'$, $E_G' - E_Y'$, and $E_B' - E_Y'$ are matrixed with the luminance signal E_Y' in the video output stage. The color signals from the video outputs, E_R' , E_G' , and E_B' , are applied to the three cathodes of the picture tube.

The signal processing in the R-G-B system consists of AGC and sync separator circuits, shown in Fig. 2. A buffer stage, Q_1 , is located on the video IF amplifier board and provides both a low impedance video output from the emitter and an inverted video signal from the collector.



Sync separation is achieved by Q_5 which provides an output capability of 50 volts peak-to-peak. Q_4 is an emitter follower driver stage providing the desired low impedance drive for Q_5 . Noise cancellation in the sync separator circuit is achieved by Q_3 . If a negative noise pulse exists during the video period, Q_2 will act as a normal amplifier. Q_3 will conduct when the base voltage exceeds the V_{BE} threshold and a negative pulse will be generated at the base

The graph plots AGC Voltage in Volts on the y-axis (0 to 10) against Input Signal Level in -10 Volts on a logarithmic x-axis (10 to 1000K). Two curves are shown: IF AGC Voltage and Tuner AGC Voltage.

Input Signal Level (-10 Volts)	IF AGC Voltage (Volts)	Tuner AGC Voltage (Volts)
10	4.0	1.0
100	5.5	1.1
1K	6.5	1.8
10K	6.5	3.2
100K	7.5	3.8
1000K	8.5	3.9

Fig. 3. Receiver AGC Characteristics

CHROMA AND BURST AMPLIFIERS, KILLER-ACC DETECTOR

Low level color processing circuitry is shown in Fig. 4. The response of the chroma bandpass amplifier compensates for the high frequency rolloff in the video IF amplifier to provide proper overall selectivity to the chroma subcarrier

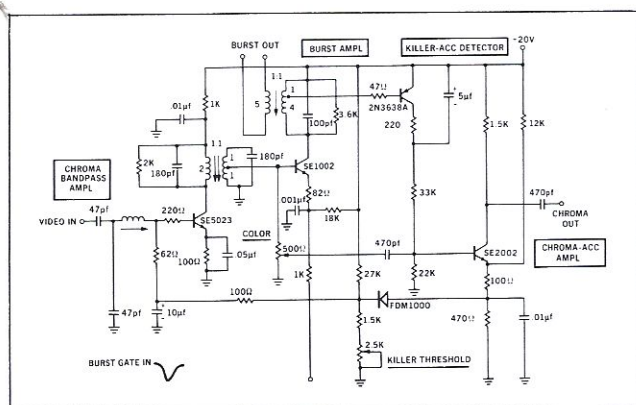


Fig. 4. Low Level Color Processing

information. (The response of a typical color television video IF amplifier is shown in Fig. 5.) There are two selectivity networks in the chroma bandpass amplifier. A single tuned circuit at the input is tuned at 4.1 megahertz and has a loaded Q of 6. A double tuned transformer in the collector is critically coupled and tuned to 3.6 megahertz. Primary and secondary coils of this transformer each have a loaded Q of 5. ACC is provided by a forward AGC transistor which is used as the chroma bandpass amplifier. The control voltage is generated in the killer-AGC detector amplified in the untuned chroma-ACC amplifier and applied

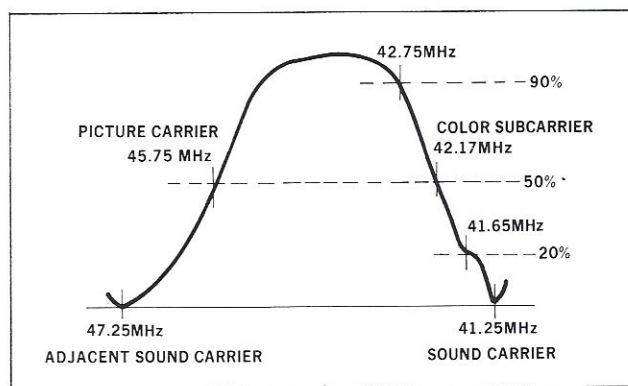


Fig. 5. Typical Video IF Amplifier Response

to the AGC transistor through a delay diode. A killer threshold control sets the maximum gain of the ACC stage. The overall response of the chroma bandpass amplifier and of the video IF amplifier to the chroma subcarrier information is shown in Fig. 6.

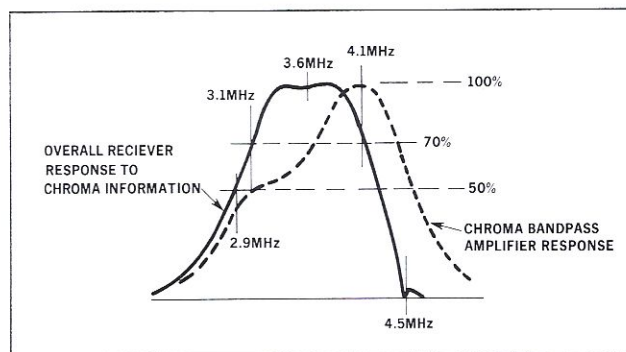


Fig. 6. Selectivity to Chroma Subcarrier Information

The output of the chroma bandpass amplifier is direct coupled to the base of the burst amplifier, which is gated "ON" during the burst period. Gating is achieved by applying a delayed negative horizontal flyback pulse to the emitter resistors of the burst amplifier transistor. A 3.6-MHz tuned transformer, with a loaded Q of 6, is used to couple the burst from the collector of the burst amplifier into the injection locked oscillator. The burst level at the transformer secondary is 5 volts peak.

The killer-ACC detector transistor is operated from the primary of the burst transformer. A burst amplitude of 1 volt peak at the tap on the transformer primary pulses the detector transistor into conduction during the burst period. The control voltage developed across the filter capacitor of the killer-ACC detector rises positively and turns on the chroma-ACC amplifier. Once the ACC delay diode comes

into conduction, the burst amplitude (as well as the chroma level) will be held essentially constant by the ACC loop.

INJECTION LOCKED CRYSTAL REFERENCE OSCILLATOR AND QUADRATURE AMPLIFIER

The injection locked oscillator shown in Fig. 7 uses the $\mu A703E$ integrated circuit which has been designed for limiter-amplifier and oscillator applications. The inductor, L_1 , in combination with the series capacitors, C_1 and C_2 , make up the reactive components of the temperature-compensated 3.6-MHz output tank circuit. The 1.5-volt peak-to-peak oscillator output, which is taken from the capacitive divider (C_1 and C_2) is primarily established by the loading placed across the inductor, L_1 . The loaded Q of the output tank is approximately 5. The inductor, L_1 , provides a ± 400 -Hz oscillator frequency adjustment range with less than a 1-dB change in output level. This range is more than sufficient to accommodate the tolerances of all frequency determining components; the most predominant one being the ± 0.005 percent crystal in the feedback circuit.

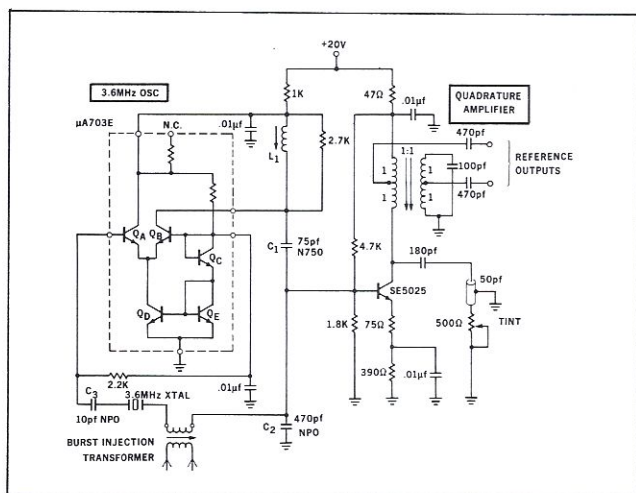


Fig. 7. Color Reference Regeneration

Positive feedback voltage to start and sustain oscillations is taken from a capacitive tap in the tuned circuit at the collector of transistor Q_B . This voltage is fed back through a narrow bandpass filter to the base of transistor Q_A . The common-collector transistor, Q_A , drives the common-base transistor, Q_B , to complete the regenerative feedback path required for oscillation.

The crystal in the feedback loop is the primary frequency-determining element. It operates in an inductive mode and resonates with capacitor C_3 . The burst injection transformer induces the chroma reference synchronizing voltage into the feedback loop of the oscillator. The oscillator will tend to lock to the induced synchronizing voltage if the ratio

of induced voltage to feedback voltage is large and the frequency difference between the oscillator and induced voltage is small. These two factors will further influence the phase relation between the oscillator and the reference burst in the locked condition.

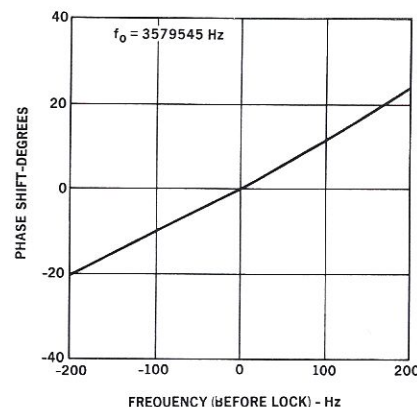


Fig. 8. Phase Shift as a Function of Oscillator Free-Running Frequency

It has been found by controlled viewing tests of color scenes that the maximum tolerable phase error in the chrominance signal (or in the regenerated color reference signal) is approximately ± 15 degrees.¹ For the injection locked oscillator in Fig. 7, a normal injection level (5 volts peak) will hold the phase error of the locked oscillator to within ± 15 degrees for a 100-Hz change in the oscillator free-running frequency. (See Fig. 8.) Since measured oscillator drift due to all causes is considerably less than 100 hertz, as shown in Figs. 9 and 10, the expected tint shift in normal set operation would be quite acceptable. Pull-in capability of the circuit with a normal injection level is ± 400 hertz.

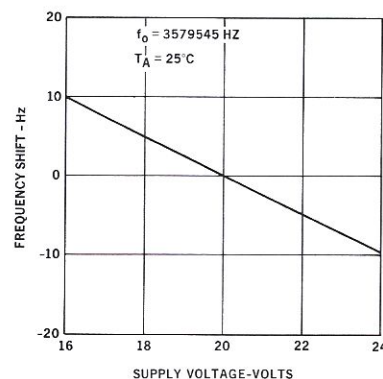


Fig. 9. Oscillator Frequency versus Supply Voltage

The quadrature amplifier, which serves as a buffer to the oscillator, develops 3-volt, peak-to-peak, quadrature reference signals from the primary and secondary of the double-tuned, loosely coupled transformer. A tint control,

which is part of the primary tuning, provides a phase adjustment range of 100 degrees.

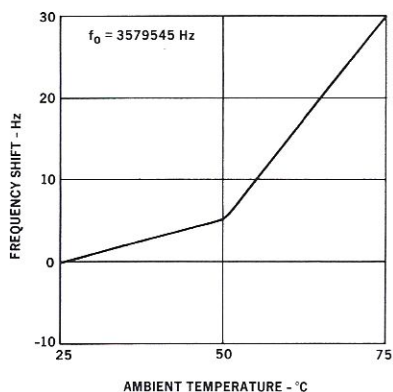


Fig. 10. Oscillator Frequency versus Ambient Temperature

CHROMA DEMODULATOR

The chroma demodulator has been designed as a monolithic integrated circuit. Because of the economics of IC's, the liberal use of transistors and resistors is applicable. To keep packaging costs low, the number of connections to the circuit have been minimized. The excellent component matching which can be achieved on a single silicon chip is heavily relied upon in the design of the demodulator.

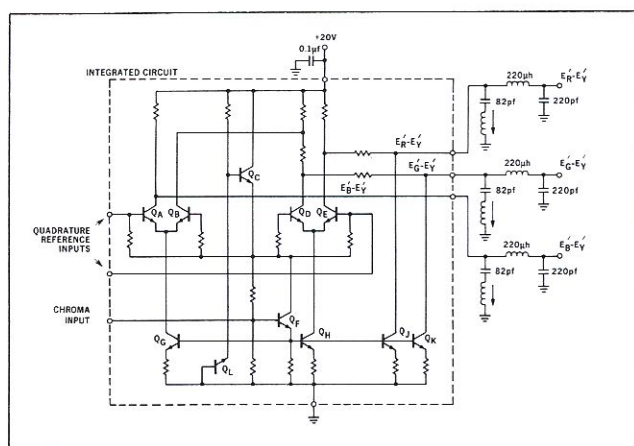


Fig. 11. Chroma Demodulator

A schematic of the integrated circuit chroma demodulator is shown in Fig. 11. Chroma is fed through the emitter follower, Q_F , to the bases of the four transistors, Q_G , Q_H , Q_J , and Q_K . Two of these four transistors, Q_G and Q_H , are high impedance chroma drives to the two transistor switches made up of the emitter coupled pair, Q_A and Q_B , and of the pair, Q_D and Q_E , respectively. The other two transistors, Q_J and Q_K , are for d.c. level shifting only.

The emitter coupled transistor switches are operated by the two reference inputs from the quadrature amplifier. Chroma current is switched between the two transistors of each emitter coupled pair. Color difference voltages, $E'_B-E'_Y$ and $E'_R-E'_Y$ are developed across the collector resistors of Q_A and Q_E , respectively. Collector currents from Q_B and Q_D are added in a resistor matrix to develop the color difference voltage, $E'_G-E'_Y$.

Because of the relative gains required in the demodulation process, the collector resistors are not equal. The output impedances for the three color difference signals are made equal by adding resistance between the collectors of Q_D and Q_E and the outputs $E'_G-E'_Y$ and $E'_R-E'_Y$, respectively. The d.c. voltages at the three outputs are made equal (under the condition of no chroma input) by adding an appropriate value of direct current from Q_J and Q_K through the resistor networks associated with the $E'_R-E'_Y$ and $E'_G-E'_Y$ outputs.

A regulated supply within the demodulator includes transistor Q_C and the zener-connected transistor Q_L .

A series trap tuned to 3.6 megahertz and a low pass filter are connected to each of the color difference outputs to remove unwanted high-frequency components generated in the demodulation process.

LUMINANCE AMPLIFIERS, MATRIX-VIDEO OUTPUTS

The luminance amplifier, matrix, and video output circuitry is shown in Fig. 12. Negative sync video from the video buffer stage is applied to the first luminance amplifier. Video peaking networks in both the base and emitter of the amplifier increase the rise time and introduce overshoot into the pulse response characteristics of the luminance channel. Fig. 13(a) shows a VITS (vertical interlace test signal) pulse at the output of the IF detector buffer. Fig. 13(b) shows the same test pulse at the collector of the first luminance amplifier after peaking. The

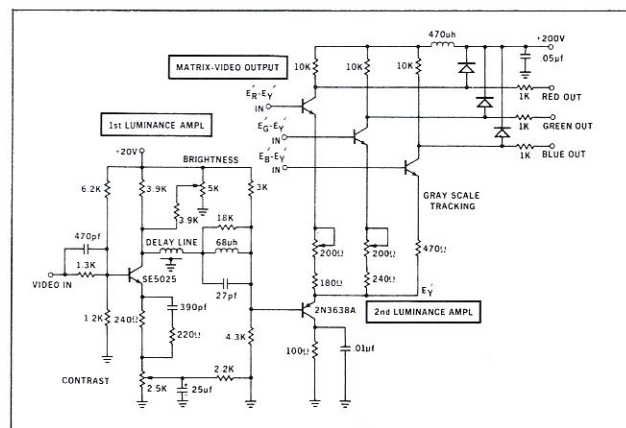


Fig. 12. Luminance Amplifiers and Matrix-Video Output

contrast control provides partial d.c. coupling above the minimum contrast setting.

The delay line in the collector of the first luminance amplifier is terminated in its characteristic impedance ($Z_0 = 2\text{ k}\Omega$) at both ends. The series inductance at the delay line output is necessary for compensating the non-uniform delay properties of the line. A capacitor in parallel with this inductor forms a trap to the chroma subcarrier frequencies. The brightness control changes the d.c. voltage operating level of the collector of the first luminance amplifier, but has a minimal effect of the driving impedance to the delay line.

The second luminance amplifier is simply an emitter following buffer between the delay line and the video output stage. Power dissipation in the buffer transistor is reduced by placing a resistor between its collector and ground. VITS patterns of frequency and pulse responses at the emitter of the second video amplifier are shown in Fig. 14(a). The preshoot in the pulse response is introduced by the delay line.

Pre-picture tube matrixing and high-level video drive are achieved in a simple three-transistor circuit. Color difference signals, $E_R' - E_Y'$, $E_G' - E_Y'$, and $E_B' - E_Y'$ are applied to the bases of the three output transistors, whereas the luminance signal, E_Y' , is applied in common to the resistors that connect to the emitters of these three transistors. Color signals E_R' , E_G' , and E_B' are developed across each of the emitter resistors. The color signal currents developed in each of the emitter resistors flow from the collectors of the output transistors into large collector resistors. The high-level color signals developed across these resistors are applied to the cathodes of the picture tube. The collector resistors are returned to a single coil for peaking of the high-frequency luminance information which is common to all three outputs. A resistance-diode network is included in each of the outputs for device protection

against picture tube arcing. The relative gains of each of the video outputs is adjusted with the gray scale tracking controls. These controls, when properly adjusted, also set up correctly compensated color drive for best color fidelity regardless of relative phosphor efficiencies of the picture tube. (It is assumed that the angles of demodulation and the gains in the chroma demodulator have been based on the color properties of the particular phosphors used in the picture tube.²)

VITS patterns of frequency and pulse response at the "BLUE" cathode of the picture tube are shown in Fig. 14(b).

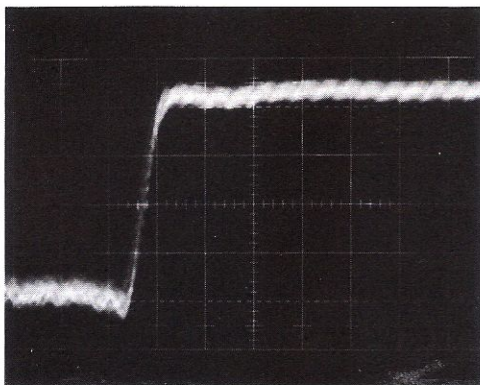
CONCLUSION

Semiconductor circuits have been described for the R-G-B system of color processing. A number of advantages have been listed for this system; (1) lower cost because of fewer and less expensive components; (2) improved performance because of improved luminance output response and because of automatic color compensation with gray scale tracking; (3) excellent reliability because of the arc protection that the R-G-B system offers to the video output devices.

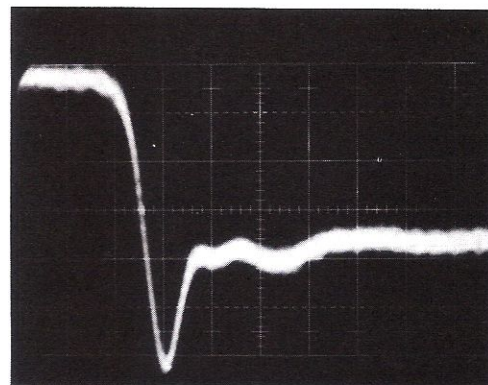
Integrated circuit concepts have been introduced into the system where there are potential economic and performance advantages. The particular integrated circuits described could be produced with semiconductor device fabrication capabilities that, in the future, will be geared to high-volume, low-cost production.

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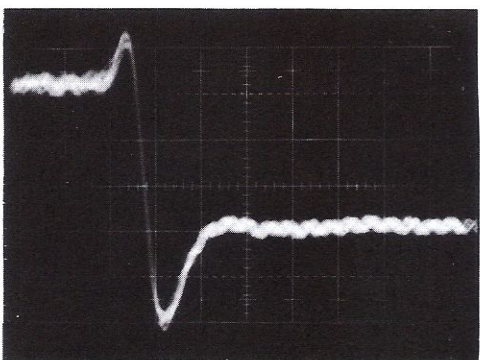


0.5V/DIV, 0.5 μ s/DIV
(a) Video buffer output



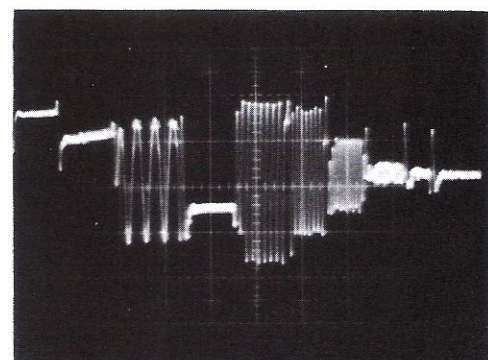
1V/DIV, 0.5 μ s/DIV
(b) Collector of first luminance amplifier

Fig. 13. VITS Pulse Response

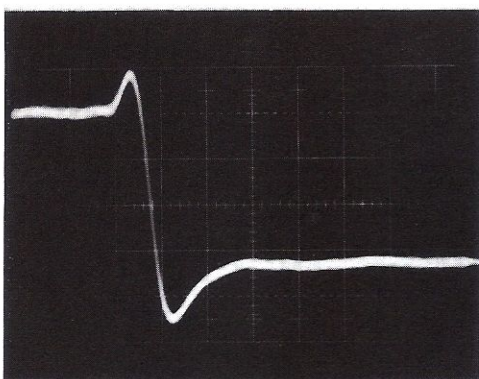


1V/DIV, 0.5 μ s/DIV

(a) Emitter of second luminance amplifier

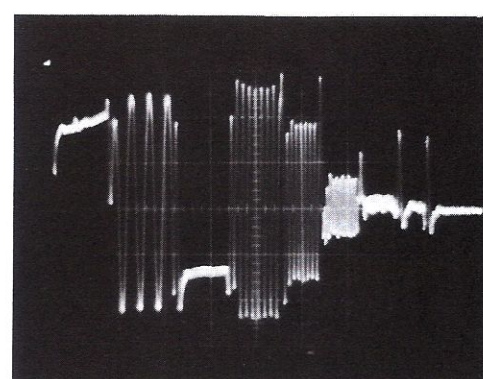


2V/DIV, 5 μ s/DIV



20V/DIV, 0.5 μ s/DIV

(b) "BLUE" cathode



20V/DIV, 5 μ s/DIV

Fig. 14. VITS Pulse and Frequency Responses

